

Implementation of AMBA Based AHB2APB Bridge

Bhagvati Panchal, Yogesh Parmar, Haresh Suthar

Abstract: The Advance Micro controller Bus Architecture bus protocol is used to build high performance SoC designs (system on chip). This achieves communication through the connection of different functional blocks (or IP). By using multiple controllers and peripherals, it makes possible to develop multiprocessor unit. It provides reusability of IP of different buses of AMBA, which can reduce the communication gap between high performance buses and low speed buses. To perform high-speed pipelined data transfers, AMBA based embedded system becomes a demanding hypothesis analytical wise, by using different bus signals supported by AMBA. To synthesize as well as simulate the composite annexation which connects advance high performance bus and advance peripheral bus which known as AHB2APB Bridge in addition to no data loss during transfer is the main target of this work. Implementation of bridge module is designed in Verilog HDL and functional and timing simulation of bridge module are done on a platform of Xilinx.

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Keywords: *Pipelined Data, SOC, Synthesis, Simulation, Verilog HDL, Handshaking Signal, AMBA.*