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Reduction of Test Time using Multiple Test Control Point Insertion for 7nm Technology Node

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Abstract*: *Test time reduction is a prominent challenge in scan based Design For Testability (DFT) architectures for cost effective test. Reliability and testability both are main objectives for DFT in today's VLSI design. In this paper, we have proposed multiple standard test control point insertion technique for 7nm technology node. The design was tested on 7828 sequential cells. We have compared results of following three Design Rule Check (DRC) (1) Scan DRC (2) Clock Scan DRC (3) Multiple standard test control point insertion DRC. We have used software tool Synopsys TetraMAX ATPG, Synopsys DFTMAX and Synopsys DFT compiler to verify the design. It has been observed that multiple standard test control point insertion DRC takes minimum time to check design of 7828 sequential cells.

Keywords* : *DRC, Scan insertion, DFT, VLSI.