Design and Analysis of Ring Oscillator CMOS circuit at 65 nm Technology

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Abstract: The Ring oscillator is a very compact device compared to other oscillators. There are many advantages of ring oscillator i.e. contain the low area, high speed. A ring oscillator is a device composed of an odd number of NOT gates, the output of these not gates oscillates between two different voltage levels, representing logic 1 and logic 0. The NOT gates or inverters are connected in a series and the output of the last inverter is fed back into the first. This paper presents CMOS ring oscillator designed for low power application using 65 nanometers (nm) CMOS technology. This design can be used for low frequency and high frequency for sampling in random number generator circuits. The proposed design having average power is 25 nanowatt at the supply voltage of 1 volt and consumes low power as compared to existing designs.

Key index: CMOS low power, Cadence virtuoso, Ring oscillator.