REDUCTION OF TEST TIMEDURING DESIGN FOR TESTABILITY

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by

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ABSTRACT

As VLSI technology is continuously shrinking to lower technology nodes we need efficient technique for testing. Now, reliability and testability both are the important parameters in today's VLSI design. Reducing the testing time is major challenge in scan based DFT (or test) the sequence that, when applied to a digital circuit, it will enables automatic test equipment to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects. Now, ATE machines are very expensive machine i.e. (i) more number of test patterns will take more time to execute and that result in more cost. (ii) more data architecture for cost-effective test. So, more pattern volume will require more storage capacity. Larger pattern volume need more time for scan operation in DUT also. DFT Compiler from Synopsys is used to generate the verified scan design. ATPG tool generate vectors that can detect volume needed more memory to store, that will result in more cost. The ATPG tool generates a statistics report later that tells us what the tool has done and provides fault category information that we have to interpret to debug coverage problems. Test-time improvement by reordering the scan cells as per priority is the main focus of this dissertation. I achieved significant DFT-debugging time of 19.56% with compare to normal scan operation by adding STCPI and reordering the scan chains.