Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech. Summer 2018 - 19 Examination

Semester: 2 **Date: 10/05/2019**

Subject Code: 203212180 **Time: 10:30 AM TO 1:00 PM**

Subject Name: Program Elective-III VLSI Circuits Testing & Verification **Total Marks: 60**

Instructions:

1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 **A)** Explain FPGA Design Flow. **(05)**

B) Write difference between Verification and Testing. **(05)**

C) Explain Types of Testing. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**

A) Explain Levels of Testing.

B) Explain the following terms.

I. Defect

II. Error.

III. Fault.

C) Write difference between Verilog and system Verilog.

D) Discuss Single Stuck-at Faults with suitable example.

Q.3 **A)** Write Verilog code of a 4 to 1 multiplexer using data flow, behavior, and structural types of modeling. **(07)**

B) Explain the following terms. **(08)**

I. Black Box verification.

II. White Box verification.

III. Gray Box verification.

OR

B) Write Verilog code and test bench of full adder circuit. **(08)**

Q.4 **A)** Draw and explain JTAG Architecture. **(07)**

OR

A) Explain Verification flow. **(07)**

B) What is Automatic Test Equipment (ATE)? Draw and explain block diagram of ATE. **(08)**