Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech. Summer 2018 - 19 Examination

Semester: 2 **Date: 08/05 /2019**

Subject Code: 203212152 **Time: 10:30 AM TO 1:00 PM**

Subject Name: CMOS Circuit Design-II **Total Marks: 60**

Instructions:

1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 A) With neat sketch Explain the schematic, internal structure and working of DRAM. **(05)**

B) What are the general consideration for reference voltage or current and explain supply independent biasing. **(05)**

C) With neat sketch, explain current mirror circuit. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**

A)What is Flash ADC? Explain 3 bit Flash ADC with neat diagram.
B) Draw and Explain CMOS Inverter Layout steps.
C) Explain charge pump PLL.
D) Explain Floating memory and Erasable Memory with neat diagram.

Q.3 A) Find the number of input combinations, values for 1 LSB, the percentage of accuracy and Full scale voltage , for 3 bit , 8 bit, 16 bit DAC and Vref= 5V. **(07)**

B) Explain PLL with neat diagram and draw the waves for phase difference 0, 90 and 180 degree. **(08)**

OR

B) Explain Open Array Architecture and Folded Array Architecture, with neat diagram. **(08)**

Q.4 A) Explain global decoder and local decoder of memory array architecture . **(07)**

OR

A) Derive the equation of positive TC and negative TC. **(07)**

B) Design 3 bit Resistor string DAC, having Vref=5V, Power Dissipation =5mW and take any digital input of 3 bit and find Analog output voltage according to input. **(08)**