Seat No: _____ Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech., Summer 2017 - 18 Examination

Semester: 2 **Date: 25/05/2018**
Subject Code: 03212180 **Time: 02:00 pm to 04:30 pm**
Subject Name: Vlsi Circuits Testing and Verification **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 A) ASIC Design Flow. **(05)**

B) Difference between Verification vs. Testing. **(05)**

C) Explain Types of Testing. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**

A) Explain Levels of Testing.

B) Explain the following terms.

I. Defect

II. Error.

III. Fault.

C) Difference between Verilog and system Verilog.

D) Discuss Single Stuck-at Faults with suitable example.

Q.3 A) Write Verilog code for Implementation of a 4 to 1 Multiplexer Using Data Flow , Behavior & Structural types of modeling. **(07)**

B) Explain the following terms. **(08)**

I. Black Box verification.

II. White Box verification.

III. Gray Box verification.

OR

B) Write Verilog code & test bench of Full Adder circuit. **(08)**

Q.4 A) Draw and Explain JTAG Architecture. **(07)**

OR

A) Explain Verification flow. **(07)**

B) What is Automatic Test Equipment (ATE)? Draw & Explain Block diagram of ATE. **(08)**