Seat No: _____ Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech., Summer 2017 – 18 Examination

Semester: 2 **Date: 21/05/2018**
Subject Code: 03212152 **Time: 2:00 pm to 4:30 pm**
Subject Name: Cmos Circuit Design-II **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 A) With neat sketch explain the basic architecture of DRAM. **(05)**

B) Draw the basic circuit of a switched capacitor, its equivalent circuit, explain its operation and derive its equivalent resistor value. **(05)**

C) Describe basic PLL topology. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**

A) Explain detail procedure for input matching using LNAS.

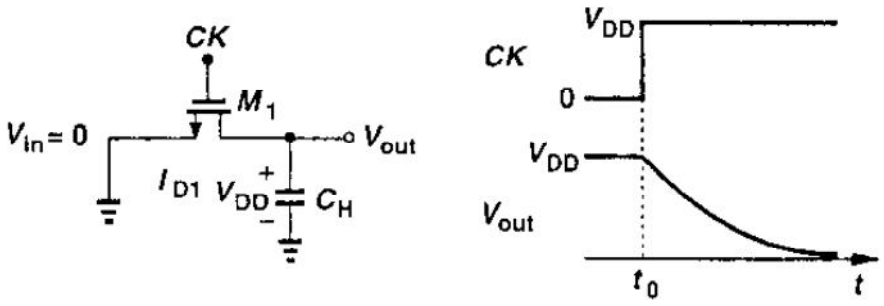
B) What is a flash converter? Discuss the working of a 3-bit flash A/D Converter.

C) Explain delay locked loops in PLLs.

D) Design unit gain sampler circuit using Op-amp.

Q.3 A) Design start up circuit for band gap reference. **(07)**

B) Calculate Vout for the given circuit. Assume $\lambda = 0$. **(08)**



OR

B) A type- I PLL experiences a frequency step $\Delta\omega = 0$ at $t = 0$.Calculate the change in phase error. **(08)**

Q.4 A) Explain PTAT current generator circuit. **(07)**

OR

A) Design pre amplification stage of comparator using NMOS and PMOS. **(07)**

B) Give detail about MOSFET as a complementary switch with circuit diagram. **(08)**