Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech. Winter 2018 - 19 Examination

Semester:1 **Date:13/12/2018**
Subject Code: 203212133 **Time: 10:30am to 01:00pm**
Subject Name: Digital VLSI Design **Total Marks: 60**

Instructions:

1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 A) Compare CPLD and FPGA. **(05)**
B) Explain ASIC Design flow. **(05)**
C) Explain Design Methodology in detail. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**
A) Discuss Semi-Custom ASICs.
B) What is Delta-delay? What is its effect in VHDL?
C) Write VHDL code for 8 x 1 MUX circuit using Behavioral, Structure and data flow modeling.
D) Write Difference between VHDL & VERILOG.

Q.3 A) Explain Process statement. Explain the importance of sensitivity list. Quote suitable example. **(07)**
B) Draw and Explain CPLD Architecture. **(08)**

OR

B) Explain various versions of wait statements with appropriate example. **(08)**

Q.4 A) Explain transport delay model with suitable example. Also summaries effect of transport delay on signal drivers. **(07)**

OR

A) Write the VHDL code for the 3 to 8 decoder using behavioral style of modeling. **(07)**
B) Explain different types of modeling methods in details with examples. **(08)**