Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

M.Tech. Winter 2019 - 20 Examination

Semester:3 **Date:26-11-2019**
Subject Code: 203212232 **Time:10:30am to 01:00pm**
Subject Name: FPGA Digital Design **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 A) Difference between PAL & PLA. **(05)**
B) Explain Front end Design & Back end Design. **(05)**
C) Difference between Mealy model & Mealy model. **(05)**

Q.2 **Answer the following questions**. (Attempt any three) (Each five mark) **(15)**
A) Discuss Xilinx 4000 series FPGAS.
B) Explain Clocking Methods & Clocking strategy in ASIC Design.
C) Explain Programmable interconnects in Xilinx 3000 series FPGAS.
D) Discuss Semiconductor Manufacturing process.

Q.3 A) Discuss Altera complex CPLD. **(07)**
B) Considering the following Boolean functions design a combinational circuit using a PAL:
w (A B C D)= $\sum$(1,3,4,6,9,11,12,14)
x (A B C D)= $\sum$(1,3,4,6,9,11,12,14,15) **(08)**
y (A B C D)= $\sum$(0,2,4,6,8,12)
z (A B C D)= $\sum$ (2,3,8,9,12,13)

OR

B) Design 12:1 mux using 4:1 multiplexers. Explain truth table of circuit. **(08)**

Q.4 A) Implement full subtractor using 1:8 Demultiplexer. **(07)**

OR

A) Discuss Xilinx 3000 series FPGAS Logic Cell Array. **(07)**
B)Design BCD to Excess-3 code converter & Implement using PLA. **(08)**