Seat No:_____ Enrollment No:_____

PARUL UNIVERSITY

FACULTY OF APPLIED SCIENCE

B.Sc /IMSC. Winter 2017-18 Examination

Semester: 3 **Date: 23/12/2017**
Subject Code: 11104201 **Time: 10.30 am to 1.00 pm**
Subject Name: Electronics **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1. A) Essay type (Each of 04 marks) **(08)**
(a) Discuss AND, OR, NOT, NAND and NOR logic gates along with their truth table, symbol and expression.
(b) Briefly discuss De Morgan's theorems with truth table and suitable diagrams using gates.

Q.1. B) Answer the following questions (Any two)
(a) Define the below given terms in brief with their suitable electric circuits and give the expression of ripple factor of both the terms justifying their efficiency to convert ac into dc. **(04)**
1.Half Wave Rectifier
2.Full Wave Rectifier
(b) Write all the Boolean laws in tabular form. **(04)**
(c) Give the working idea of solar cell. **(04)**

Q.2. A) Answer the following questions.
(a) Discuss the below given terms in brief with their suitable diagrams. **(04)**
1. Forward bias of PN junction diode.
2. Reverse bias of PN junction diode.
(b) Graphically represent the forward and reverse characteristics of PN junction diode in forward and reverse biasing respectively and give physical representation of them as well. **(04)**

Q.2. B) Answer the following questions (Any two)
(a) Multiple choice questions. **(03)**
1. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):
a) AND b) NAND c) NOR d) OR
2. GATE that is an inverter is called as
a) OR b) NOT c) XOR d) NAND
3. A semiconductor has generally _____ valence electrons.
a) 2 b) 3 c) 6 d) 4
(b) Give a brief view on idea of biasing in semiconductor **(03)**
(c) Explain diode resistance in detail. **(03)**

Q.3. A) Essay type (Each of 04 marks) **(08)**
(a) Give a brief idea on qualitative mechanisms of junction breakdowns.
(b) Give a detail view on barrier potential.

Q.3. B) Answer the following questions (Any two)
(a) Short note/ Brief note (Each of 02 marks) **(04)**
1. Discuss about a transition capacitance.
2. Explain Zener diode schematically.
(b) With the help of label diagram explain barrier formation. **(04)**
(c) Define: drift current, diffusion current, Fermi level, energy band in semiconductor. **(04)**

Q.4. A) Answer the following questions.
(a) Short note/ Brief note (Each of 02 marks) **(04)**
1. Give a brief view on electrical conductivity.
2. Short note on Fermi level of extrinsic semiconductor.
(b) Write in detail about dependence of Fermi level on donor and acceptor concentration. **(04)**

Q.4. B) Answer the following questions (Any two)
(a)Multiple choice question (Each of 01 marks) **(03)**
1. The majority charge carriers in a p type semiconductor are
a) Holes b) Electrons c) Both d) None of them
2. Fermi level for extrinsic semiconductor depends on
a) Donor element b) Impurity concentration c) Temperature d) All

3. Mobility of holes is _____ mobility of electrons in intrinsic semiconductor.

a) Equal b) Greater than c) Less than d) can not define

(b) Answer in detail about energy bands in solids. **(03)**

(c) Discuss in detail about carrier mobility. **(03)**