Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech Mid Semester Exam JAN-FEB 2024

Semester: 6th **Date: (01/02/2024)**

Subject Code: (203122383) **Time: (1hr: 30min)**

Subject Name: (Real Time Embedded Systems) **Total Marks: 40**

Sr. No.		Marks
Q.1	(A) Five One-line Questions (i) What is the primary goal of optimizing design metrics in embedded systems? (ii) List the common design challenges in embedded systems? (iii) What does the term "real-time constraints" refer to in embedded systems? (iv) Which design metric is focused on the responsiveness and predictability of an embedded system? (v) In the context of embedded systems, what does the term "power consumption" refer to?	05
	(B) Five Fill in the blanks (i) _____is the key consideration when optimizing for low power consumption in embedded systems. (ii) Reliability is crucial in embedded systems due to _____. (iii) _____is an effective approach to optimize cost in embedded systems design. (iv) How effectively system resources are used to perform tasks in the context of embedded systems is called _____. (v) _____ is a trade-off that designers often face in optimizing embedded systems.	05
Q.2	Attempt any four (Short Questions)	12
	(1) With the help of an example explain," what is embedded system?"	
	(2) State different design metrics used while designing an embedded system.	
	(3) What is general purpose processor? Explain.	
	(4) Draw the block diagram of a single purpose processor.	
	(5) What is design technology? Explain.	
Q.3	Attempt any two questions	08
	(1) Enumerate the functions of timer, counter and watchdog timers.	
	(2) Explain the steps of combinational circuit design.	
	(3) Explain the steps of sequential circuit design	
Q.4	(A) Compulsory	05
	(B) y is 1 if a is equal to 1, or b and c is equal to 1. z is 1 if b or c is equal to 1, but not both. Design a combinational circuit for the problem statement.	05
	OR	
	(B) You want to construct a clock divider. Slow down your pre-existing clock so that you output a 1 for every four clock cycles. Draw the state diagram and truth table and design the sequential circuit.	05