Semester: 6
Subject Code: 203105428.
Subject Name: High Performance Computing

Date: 31/01/2024
Time: 1hr: 30min
Total Marks: 40

Sr. No.		Marks

Q.1 **(A) One-line Questions** — Marks 5

i) What is the primary motivation for parallel computing?
ii) Name two types of parallel programming models discussed in the syllabus.
iii) Define SIMD architecture.
iv) What are the basic building blocks in message-passing programming?
v) Explain the term "load balancing" in the context of parallel algorithm design.

(B) Five Fill in the blanks — 05

i) _____ is a limitation of memory system performance in parallel computing platforms.
ii) In the context of parallel algorithm design, _____ involves dividing a problem into smaller sub-problems.
iii) _____ and _____ operations are fundamental building blocks in message-passing programming.
iv) The dichotomy of parallel computing platforms involves _____ and _____ platforms.
v) N-wide superscalar architectures and multi-core are examples of parallel computing _____.

Q.2 **Attempt any four (Short Questions)** — 12

(1) Describe three levels of parallelism in the context of parallel computing.
(2) Explain the principles of load balancing in parallel algorithm design.
(3) Discuss the limitations of memory system performance in parallel computing platforms.
(4) Outline the characteristics of tasks and interactions in parallel algorithm design.
(5) Differentiate between SIMD and MIMD architectures, providing examples of each.

Q.3 **Attempt any two questions** — 08

(1) Explain the principles of message-passing programming, highlighting its importance in parallel computing.
(2) Detail the mapping techniques used for load balancing in parallel algorithm design.
(3) Compare and contrast multi-core and multi-threaded architectures in parallel computing.

Q.4 (A) Discuss the trends in microprocessor architectures and their impact on parallel computing. — 05

(B) Design a parallel algorithm for a specific problem, considering decomposition techniques and load balancing. — 05

OR

(B) Demonstrate the steps involved in basic CUDA programming, emphasizing its significance in high-performance computing. — 05