Seat No: _____ Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech. Winter 2022 - 23 Examination

Semester: 3 **Date: 11/10/2022**
Subject Code: 203107203 **Time: 2:00pm to 4:30pm**
Subject Name: Digital System design **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 Objective Type Questions **(15)**

1. Which of the following is an example of a digital Electronic?
a) Computers b) Information appliances c) Digital cameras d) All of the mentioned
2. Which of the following is a type of digital logic circuit?
a) Combinational logic circuits b) Sequential logic circuits c) Both a & b d) None of the mentioned
3. Which of the following options comes under the non – saturated logic family in Digital Electronics?
a) Emitter – coupled Logic b) High-Threshold Logic
c) Integrated – injection Logic d) Diode – Transistor Logic
4. Which characteristic of IC in Digital Circuits represents a function of the switching time of a particular transistor?
a) Fan – out b) Fan – in c) Power dissipation d) Propagation delay
5. Which of the following digital logic circuits can be used to add more than 1 – bit simultaneously?
a) Full – adder b) Ripple – carry adder c) Half – adder d) Serial adder
6. What is the BCD adder?
7. Write the full form of SOP.
8. For n=2 variables, total no. of possible involved min-terms in the K-map?
9. Define the signal?
10. How many inputs are in Full-Adder?
11. BCD code is the _____bit code. (Choose right answer 1, 2, 3, 4)
12. Full form of TTL is _____.
13.for S-R Flip Flop, if S=0 and R=0, then Q(t) will be _____
14. Size of the encoder is _____.
15. For n=3 variables, total no. of selection line in the MUX is _____.

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) Design NOT, AND & OR gate using NAND gate?
B) Design Full Adder logic circuit.
C) Design the J-K Flip flop with characteristics table.
D) Define the shift registers and its types.

Q.3 A) Design NOT & AND gate using $2X1$ Multiplexer. **(07)**

B) $f\ (A, B, C) = \sum m\ (3,5,6,7)$ for given function, minimize the expression and identify the: Implicants (I), Prime Implicants (PI), and Essential prime implicants (EPI). **(08)**

OR

B) What is the race-around condition? How it can be removed? Define with proper diagram. **(08)**

Q.4 A) Explain the working of TTL NAND gate with logic circuit. **(07)**

OR

A) Define the different modeling styles in VHDL. **(07)**
B) Design the CMOS inverter and their working. **(08)**