PARUL UNIVERSITY
FACULTY OF ENGINEERING \& TECHNOLOGY
B.Tech. Winter 2022-23 Examination

Semester: 3
Subject Code: 203106207
Date: 11/10/2022
Subject Name: Analog \& Digital Electronics
Time: 2:00pm to 4:30pm
Total Marks: 60

## Instructions:

1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.
Q. 1 Objective Type Questions - (All are compulsory) (Each of one mark)
5. Which number system has a base 16
A. Hexadecimal
B. Binary
C. Octal
D. Decimal
6. How many entries will be in the truth table of a 4 -input NAND gate?
A. 8
B. 16
C. 32
D. 4
7. How many bits are needed to store one BCD digit?
A. 1
B. 2
C. 4
D. 8
8. Which of these sets of logic gates are known as universal gates?
A. XOR, NAND, OR
B. OR, NOT, XOR
C. NOR, NAND
D. NOR, NAND, XNOR
9. In the toggle mode, a JK flip-flop has
A. $\mathrm{J}=0, \mathrm{~K}=0$
B. $\mathrm{J}=0, \mathrm{~K}=1$
C. $\mathrm{J}=1, \mathrm{~K}=0$
D. $\mathrm{J}=1, \mathrm{~K}=1$
10. The following hexadecimal number (1E.43)16 is equivalent to
11. Convert (312)8 into decimal
12. What is the addition of the binary number $101001+010011$
13. 1's complement of 1011001 is
14. 2's complement of 1011011 is
15. One nibble is equal to how many bits
16. Positive integers must be represented by
17. The number of inputs in a half adder is?
18. How much input and output needed for DE multiplexer?
19. What is the radix of the octal number system?
Q. 2 Answer the following questions. (Attempt any three)
A) Find The excess-3 code for 584
B) Derive DE Morgan's law
C) Explain Full Adder circuit.
D) Derive truth table for NAND gate
Q. 3 A) Design4 by 1 multiplexer.
B) Give classification of memory and explain each memory

OR
B) Explain Ideal Characteristic of op-amp.
Q. 4 A) Explain T flip flop with diagram

## OR

A) Explain Bi directional Shift Register.
B) Define following terms (1) Slew Rate (2)PSRR (3)SVRR (4)Offset voltage (5) Feedback.

