Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech. /Int. B.Tech Winter 2022-23 Examination

Semester: 3 /7 **Date: 11/10/2022**
Subject Code: 203105201 **Time: 2.00 pm to 4.30 pm**
Subject Name: Digital Electronics **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 **Objective Type Questions** - (All are compulsory) (Each of one mark) **(15)**

1. A Multiplexer with 4 select lines is a _____
   A. 4:1 MUX B. 8:1 MUX
   C. 16:1 MUX D. 32:1 MUX
2. BCD code of equivalent $(345)_{10}$ is _____
   A. 0011 1001 1010 B. 1001 1001 1111
   C. 0011 0100 0101 D. 0101 1100 1001
3. The logic expression AB+A'B' can be implemented by giving the inputs A and B to a two input
   A. X-NOR gate B. NAND gate
   C. NOR gate D. X-OR gate
4. The _____ adder speeds up the process by eliminating the ripple carry.
   A. Half adder B. Full adder
   C. BCD adder D. Look ahead carry adder
5. A Flip-flop can store _____
   A. 1 bit of data B. 2 bit of data
   C. 3 bit of data D. n bit of data
6. The 7-bit Hamming code is used to transmit _____ data bits.
7. The full form of SR is _____.
8. Full form of TTL is _____.
9. Convert Binary to Decimal to Binary number system: $(52)_{10}$ = _____
10. The numbers of row in the truth table of a 4 input gate is _____.
11. Explain the truth-table of NAND Gate with its Boolean expression.
12. Write names of universal gates.
13. Write Distributive law.
14. Find 1's and 2's complement of following binary number : $(00101101)_2$
15. Convert binary to gray code : $(1011010)_2$

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) Explain Full adder and Full subtractor.
B) Explain and Prove De-Morgan's Theorem.
C) Reduce the expression:
(1) f = A [B+C' {(AB+AC')'}]
(2) f = [(AB)'+A'+AB]'
D) Difference between Combinational circuit and Sequential circuit.

Q.3 A) What is decoder? Draw logic circuit of 3line to 8 line (3:8) decoder with truth table and explain its working. **(07)**

B) Explain 3-bit Ripple counter using JK flip-flop along with timing diagram. **(08)**

OR

B) Explain Multiplexer and Demultiplexer with details explanation of its one of type with block diagram, truth table and logic diagram. **(08)**

Q.4 A) Write Short Note on PLA. **(07)**

OR

A) Simplify Boolean function $F = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,5)$ using K-Map with Realizing circuit diagram. **(07)**

B) Explain in details NAND gate-based S-R Flipflop and D Flipflop. **(08)**