Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech. Winter 2019 - 20 Examination

Semester: 3 **Date:27/11/2019**
Subject Code: 20310307203/03107203 **Time: 02:00 pm to 04:30 pm**
Subject Name: DIGITAL SYSTEM DESIGN **Total Marks: 60**
Digital Electronics

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 Objective Type Questions - **(15)**

1.Each of the product terms in standard SOP form is called as _____.
2.The commutative laws says that_____.
3.A flip flop has _____ stable states.
4.For a J-K flip-flop , J=1 , K=1 is the _____ mode.
5.A circuit used to count the number of pulses is called a _____.
6.A multiplexer with 4 select lines is a
a) 4:1 Multiplexer
b) 8:1 Multiplexer
c) 16:1 Multiplexer
d) 32:1 Multiplexer
7.Which logic device is called as a distributor?
a) Multiplexer
b) Demultiplexer
c) Encoder
d) Decoder
8.A combinational PLD with a programmable AND array and a Programmable OR array is called a
a) PLD
b) PROM
c) PAL
d) PLA
9.When an inverter is placed between the inputs of an S-R flip-flop , the resulting flip-flop is a
a) J-K Flip-flop
b) Master –slave Flip-flop
c) T flip-flop
d) D Flip-flop
10. The minimum number of flip-flops required for a MOD-12 counter is
a) 3
b) 4
c) 6
d)12
11 .What is full subtractor?
12.Convert 011101011 in gray code.
13.Draw symbol of ExOR and ExNOR gate.
14.Define : Propagation Delay and Fan In.
15.Simplify using K-Map: $F(A,B,C,D) = \Sigma m (0, 1, 3, 4, 5, 6, 7, 13,15)$

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) What is meant by multiplexer? Explain with diagram and truth table, Operation of 4 -to-1 line multiplexer
B)State and prove Demorgan's theorems .
C) Design combinational circuits for a full adder.
D) Discuss 4 bit BCD Adder in Detail

Q.3 A) Explain J-K flip-flop with necessary logic diagram, state equation and Truth table. **(07)**

B) State operating modes of Shift register and explain any two in detail. **(08)**

OR

B) Design a counter with the following binary sequence:0,1,3,7,6,4,and repeat.(Use D flip-flop) **(08)**

Q.4 A) Explain working of TTL NAND Gate in detail. **(07)**

OR

A) State four classes of Data Objects in VHDL and explain all in brief. **(07)**

B) Write VHDL code for below mentioned problem definition: **(08)**

1) Full adder using Data flow modeling style.
2) Basic Gates using Data flow modeling style.