Seat No: _____ Enrollment No: _____

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech.Winter2019 - 20Examination

Semester: 3 **Date: 25-11-2019**
Subject Code: 203105201/03105201 **Time: 2:00pm to 4:30pm**
Subject Name: Digital Electronics **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 **Objective Type Questions** (All are compulsory) (Each of one mark) **(15)**

1. The truth table for an S-R flip-flop has how many VALID entries?
a) 1 b) 2
c) 3 d) 4
2. The sequential circuit is also called _____.
3. The binary representation of BCD number 00101001 (decimal 29) is _____.
4. It should be kept in mind that don't care terms should be used along with the terms that are present in _____
a) Minterms b) Expressions
c) K-Map d) Latches

5. The code where all successive numbers differ from their preceding number by single bit is _____.

6. The following switching functions are to be implemented using a decoder:
f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7)
The minimum configuration of decoder will be _____
a) 2 to 4 line b) 3 to 8 line
c) 4 to 16 line d) 5 to 32 line
7. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates b) XOR or XNOR gates
c) NOR or NAND gates d) AND or NOR gates
8. _____ flip-flops are required to make a MOD-32 binary counter.
9. Bidirectional shift registers can shift data either right or left.
A.True B.False
10. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n):
A.AND B.NAND
C.NOR D.OR
11. How is a J-K flip-flop made to toggle?
12. If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____.
13. Convert binary 111111110010 to hexadecimal.
14. The voltages in digital electronics are continuously variable.
A.True B. False
15. Assign the proper even parity bit to the code 1100001.
A.11100001 B.1100001
C.01100001 D.01110101

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) Find the complement of (a)A' B + C D' (b) AB +CD = 0
B) Illustrate JK Flipflop.
C) Find the hex sum of $(93)_{16}$ + $(DE)_{16}$.
D) Simplify the Boolean expression F = C(B + C)(A + B + C).

Q.3 A) Minimize function f(A, B, C, D) = ∑(0,1,2,3,5,7,8,10,12,13,15) using tabulation Method. Note that this is in decimal form. **(07)**

B) Explain 3-bit Ripple counter using JK flip-flop along with timing diagram. **(08)**

OR

B) Write short note on 4-bit (MOD-4) ring counter. **(08)**

Q.4 A) Write difference between Decoder and Demultiplexer. **(07)**

OR

A) What is a decoder? Draw the logic circuit of a 3 line to 8 line decoder and explain its Working. **(07)**

B) Minimize function F = Σ (0, 2, 4, 8, 10, 13, 15, 16, 18, 20, 23, 24, 26, 32, 34, 40, 41, 42, 45, 47, 48, 50, 56, 57, 58, 60, 61) using K-Map. **(08)**