Enrollment No.:_____

PARUL UNIVERSITY
Faculty of Engineering & Technology
B Tech Examination

Subject Name: Analog and Digital Electronic Subject Code: 203106207
Branch: EE Semester: 3th
[Date: 08/08/2022] [Time: 10:30 to 12:00] [Total Marks: 40]

Sr.No.		Marks
Q.1	(A) Compulsory question. 1. Which of these sets of logic gate are designated as universal gates? (a) NAND (b) AND (c) NOT (d) OR 2. Find 1's complement of 1011001. 3. One nibble is equal to how many bits. 4. The Inverter is ____gate. 5. What is the Boolean Expression of OR gate?	05
Q.1	(B) Reducing the following SOP Expression using K-MAP $Y=\sum m(0,1,5,9,11,13,14,15) + d(3,4,7,10)$	05
Q.2	Attempt any four(Short Questions) (1) Explain the Inverting Op-amp. (2) Convert Octal to Decimal number system.$(152.25)_8$ (3) Reduce SOP Boolean Expression using K-Map:- $Y= \sum m (0,2,4,6,7,8,10,12,13,15)$ (4) Perform Binary addition. 1 0 1 1 0 1 + 1 1 1 1 (5)Explain 1) Input offset voltage 2) Output offset voltage 3) input offset current.	12
Q.3	Attempt any two (1) Explain Ex-OR and Ex-NOR gates with Symbol, Truth table and Boolean Expression (2) Explain Op-amp as Differential Amplifier. (3)Perform Binary Subtraction using 1's Complement. $(1\ 1\ 0\ 1\ 0)_2 - (0\ 1\ 1\ 1\ 1)_2$	08

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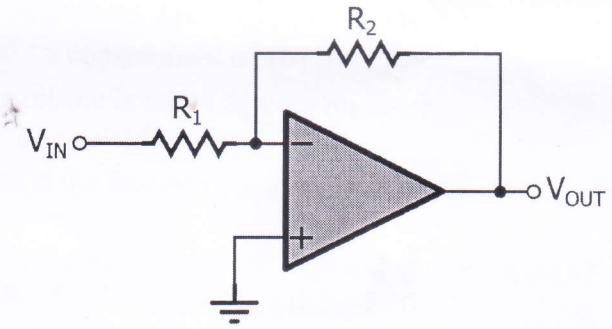
Q.4

A) Find the output Voltage of the given Op-amp, R1=10K Ohm R2=400K Ohm Vin=20 V. using KCL method 05



(B) Perform Binary Subtraction using 2's Complement. 05

$(1\,0\,1\,0\,1\,0\,0)_2 - (1\,0\,1\,0\,1\,0\,0)_2$

OR

(B). Design AND gate using NAND Gate. 05