PARUL UNIVERSITY
FACULTY OF ENGINEERING & TECHNOLOGY
B.TECH MIDSEM EXAMINATION WINTER 2021-22

SUBJECT NAME (CODE): DIGITAL ELECTRONICS (203105201)   BRANCH:CSE/IT

DATE:08/08/2022   TIME: 2:30 PM to 4:00 PM   TOTAL MARKS: 40

Sr.No.   Marks

Q.1   (A) Compulsory Question (5 MCQ)   5

1. What is Digital Electronics?
a) Field of electronics involving the study of digital signal
b) Engineering of devices that digital signal
c) Engineering of devices that produce digital signal
d) All of the mentioned

2. What is the addition of the binary number 101001+ 010011=?
a) 010100
b) 111100
c) 000111
d) 101110

3. The excess-3 code for 584 is given by
a)100010110111
b)100001110111
c)100010010110
d)100001010110

4. What will be the output of the combination of AND gate and NOT gate if the
inputs are A and B?
a) A+B
b) A*B
c) (A+B)'
d) (A*B)'

5. The gray code equivalent of (1011)2 is _____
a) 1101
b) 1010
c) 1110
d) 11ŀ1

(B) Compulsory Question (5 Fill in the Blanks)

1) Maxterm designation for A + B + C is _____.
2) TTL stands for_____
3) A Karnaugh map with 4 variables has Number of cell is _____.
4) IC number of NAND gate _____
5) Find 9's and 10's complement of decimal nos.: 3405.65

Q.2   Attempt any four(Short Questions)   12
    (1) Convert the following Numbers as directed:
        (i) (6AC)16 = ( )10 and ( )2
        (ii) (1224.125)10 = ( )8 and ( )16
    (2) Perform the operation of subtractions with the following binary numbers using 12 bit 1's complement
        (i)-89.75+43.25
    (3) Perform the operation of division and multiplication with the following binary numbers
        (i)110101.11 / 101 (ii) 1011.10*101
    (4) Demonstrate by means of truth tables the validity of the following Theorem of Boolean algebra
        (i) De Morgan's theorems for two variables
    (5) Draw the logic symbol and construct the truth table for each of the.
    [i] Two input NAND gate   [ii] Two input XOR gate
      [iii] Two input EX-NOR gate   [iv] NOT gate

Q.3   Attempt any two   08
    (1) Draw half adder and full Subtractor with neat block diagram, circuit diagram, truth table and Boolean equation.

    (2) Reduce the expression and draw the logic circuit.
        (i)   AB+ABC+A'
        (ii)   A+B(AC+(B+C')D)
    (3) Explain briefly: SOP &POS andsolve Y= **AB+AC'+BC** find it's minterm, maxterm and canonical form.

Q.4   (A) Reduce the following Boolean function using k map- **Y=Σm (0,1,5,9,13,14,15)**   05
+d (3,4,7,10,11) and draw circuit diagram.
    (B)Explain 4-bit Parallel Adder with one example **A=1010 and B= 1110.**   05
<div align="center">OR</div>
    (B) Solve the Boolean function using VEM method **Y=Σm(2,3,5,7,12,14)+d(10,11)**   05