## PARUL UNIVERSITY **FACULTY OF ENGINEERING & TECHNOLOGY**

B.Tech. Summer 2018 - 19 Examination

Semester: 6	Date: 04/05/2019
Subject Code: 03108351	Time: 10:30 AM TO 1:00 PM
Subject Name: Embedded Systems	Total Marks: 60
Instructions:	

- 1. All questions are compulsory.
- 2. Figures to the right indicate full marks.
- 3. Make suitable assumptions wherever necessary.
- 4. Start new question on new page.
- Q.1 Objective type questions (fill in the blanks, one word answer, mcq-not more than five in case of (15)mcq) (all are compulsory) (each of one mark)
  - 1. The time taken to respond to an interrupt is known as
    - a. Interrupt delay
    - b. Interrupt time
    - c. Interrupt latency
    - d. Interrupt function
  - 2. Which can activate the ISR?
    - a. Interrupt delay
    - b. Function
    - c. Procedure
    - d. Structure
  - 3. Which factor determines the cache performance?
    - a. Software
    - b. Peripheral
    - c. Input
    - d. Output
  - Which storage element is used by MAC and IBM PC? 4.
    - a. CMOS
    - b. Transistor
    - c. Capacitor
    - d. Inductor
  - 5. Which company developed I2C?
    - a. Intel
    - b. Motorola
    - c. Phillips
    - d. IBM
  - 6. \_\_\_\_\_ is the monetary cost of manufacturing each copy of the system, excluding NRE cost.
  - 7. COMS stands for\_\_\_\_\_
  - 8. The difference between the on-time and delayed triangle areas is called\_\_\_\_\_
  - 9. In digital circuit design,\_\_\_\_\_\_ is a design abstraction which models a synchronous digital circuit.
  - 10. Full form of TTL
  - \_\_\_\_\_ is the task of making design metric values the best possible. 11.
  - 12. Baud rate can define the timing in the UART.true/false
  - 13. 8250 is the most commonly used UART. Yes/no

  - 14. \_\_\_\_\_\_ helps in the generation of waveforms15. \_\_\_\_\_\_ no. of comparators present in the direct mapping cache.
- **Q.2** Answer the following questions. (attempt any three)
  - A) Explain custom single-purpose processor basic model in detail.
  - B) What are the different ways for optimizing the FSMD?
  - C) Discuss on CMOS transistor implementations.
  - D) Write a note on UART.
- **Q.3** A) Describe harvard and von neumann architecture.
  - B) Write short note on superscalar and VLIW architecture.
    - Or
  - B) List down the types of scheduling in RTOS with example.

(15)

(07)

 $(\mathbf{08})$ 

(08)

<b>Q.4</b> A) Define the following terms with example 1) timers 2) counter and 3) watchdog timers.	(07)
Or	
A) Differentiate between serial and parallel protocols.	(07)
B) What is real time operating system? Discuss rtos services and capabilities.	(08)