Seat No: _____________ **Enrollment No: ___________________**

PARUL UNIVERSITY
FACULTY OF ENGINEERING & TECHNOLOGY
B.Tech. Summer 2018 – 19 Examination

Semester: 3 **Date: 25/05/2019**
Subject Code: 03107203 **Time: 02:00pm to 04:30pm**
Subject Name: Digital Electronics **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 Objective Type Questions - (All are compulsory) (Each of one mark) **(15)**

1. Define AND Gate.
2. List out the basic gates.
3. What do you mean by truth table?
4. A NOR gate output is LOW if any of its inputs is LOW. (True/False)
5. The Boolean expression C + CD is equal to ________.
6. In 1-to-4 demultiplexer, how many select lines are required?
   a) 2
   b) 3
   c) 4
   d) 5
7. Which number system has a base of 16
   a) Decimal
   b) Octal
   c) Hexadecimal
   d) None
8. How many bits are required to store one BCD digit?
   a) 1
   b) 2
   c) 3
   d) 4
9. Which of these sets of logic gates are designated as universal gates?
   a) NOR, NAND.
   b) XOR, NOR, NAND.
   c) OR, NOT, AND.
   d) NOR, NAND, XNOR.
10. In digital systems, 1 byte is equal to ________ bit(s).
    a) 1
    b) 2
    c) 4
    d) 8
11. The radix of binary number system is ______ and the digits used are ____________.
12. In _________________________ number system 8 distinct symbols are used to specify any Number.
13. MSB = _____________________________.
14. What do you mean by sequential circuits?
15. What do you mean by combinational circuits?

Q.2 Answer the following questions. (Attempt any three) **(15)**

A) Obtain the simplified expression in sum of products for the following Boolean functions:
   a) xy + x’y’z’ + x’yz’
   b) A’B + BC’ + B’C’

B) Explain half subtractor with proper logic circuit diagram.

C) Draw a block diagram for 4 x 1 lines MUX

D) Explain De Morgan’s theorem using example.

Q.3 A) Convert the following binary numbers into octal and then to hexadecimal. **(07)**

a) 11011100.101010
b) 01010011.010101
c) 10110011

B) Simplify the Boolean expression using Karnaugh map method. **(08)**

a) $F = X'YZ + X'YZ' + XY'Z' + XY'Z$
b) $F = X'YZ + XY'Z' + XYZ + XYZ'$

OR

B) Prove the following expression **(08)**

a) $A + A \cdot B' + A \cdot B' \cdot C' + A \cdot B' \cdot C + C' \cdot B \cdot A = A$
b) $[\, 1 + L \cdot M + L \cdot M' + L' \cdot M \,] \cdot [\, (L + M') \cdot (L' \cdot M) + L' \cdot M' (L + M) \,] = 0$

Q.4 A) Design NOT gate, AND gate, OR gate and NOR gate using NAND gate. **(07)**

OR

A) Differentiate combinational and sequential circuits. **(07)**

B) Design full adder with proper logic circuit diagram. **(08)**