Seat No: _____ **Enrollment No: _____**

PARUL UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY

B.Tech. Summer 2018 - 19 Examination

Semester: 3 **Date: 29/05/2019**
Subject Code: 03105201 **Time: 02:00pmto 04:00pm**
Subject Name: Digital Logic Design **Total Marks: 60**

Instructions:
1. All questions are compulsory.
2. Figures to the right indicate full marks.
3. Make suitable assumptions wherever necessary.
4. Start new question on new page.

Q.1 **Objective Type Questions**: (All are compulsory) (Each of one mark) **(15)**

1. Any negative number is recognized by its
   a) MSB b) LSB c) Bits d) Nibble
2. The quantity of word is
   a) 16 bits b) 32 bits c) 64 bits d) 8 bits
3. 2's complement of 11001011 is
   a) 01010111 b) 11010100 c) 00110101 d) 11100010
4. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is
   a) Ex-NOR gate b) OR gate c) Ex-OR gate d) NAND gate
5. The Boolean algebra is mostly based on
   a) Boolean theorem b) De Morgan theorem c) standard theorem d)Algebraic theorem
6. _____ is the highest-value of ten -bit binary number.
7. Digital systems have _____ state.
8. Cyclic code are also called _____ code.
9. The MSB of Binary number has weight of 512, the number consist of _____ bits.
10. The digit that changes most often during counting is called the _____.
11. A logic circuit that can store one bit of information is a _____.
12. Memory devices that use electronic latching circuits are called _____.
13. The duty cycle of a square wave is _____%.
14. TTL requires a constant supply voltage of 8.0 V. True/ False
15. Pull-up resistors and pull-down resistors are used to keep a floating terminal HIGH. True/ False

Q.2 **Answer the following questions. (Attempt any three)** **(15)**

A) Explain and prove De-Morgan's theorems.
B) Prove NAND and NOR are universal gates.
C) Perform $(-4)_{10} - (-8)_{10}$ using 1's complement.
D) Minimize the expression using K-Map and realize using the basic gates.
$Y = \Sigma m(1,2,9,10,11,14,15)$

Q.3 A) Minimize expression using Tabular method. **(07)**
$Y = \Sigma m(1,5,6,12,13,14) + d(2,4)$
B) Explain D-type positive edge- triggered flip-flop in details. **(08)**

OR

B) Explain 2 bit Magnitude Comparator. **(08)**

Q.4 A) Give classification of counters and explain asynchronous 4-bit binary ripple up counter. **(07)**

OR

A) Implement 3 bit Binary to Gray converter using PLA (Programmable Logic Array). **(07)**
B) What is meant by multiplexer? Explain with diagram and truth table the Operation of 4-to-1 line multiplexer. **(08)**